#### ORIGINAL PAPER

# ISTSat-1, a space-based Automatic Dependent Surveillance-Broadcast demonstration CubeSat mission

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#### Summary

The use of space-based Automatic Dependent Surveillance-Broadcast (ADS-B) receivers to extend aircraft surveillance beyond line-of-sight communication has been discussed since the late 2000s and has been demonstrated in various missions. Although recent demonstrations have relied on small CubeSat platforms, the use of the smallest possible form factor has not been explored. This paper describes development of a spacecraft representing the first use of a 1 U CubeSat platform for aircraft tracking. To comply with the platform's limited power budget, the receiver departs from the typical application of FPGA boards to decoding ADS-B signals and instead employs a general microprocessor. The spacecraft also features some innovations over traditional CubeSat platforms, such as distributed system-level software amenable to extensive code reuse, redundant communications mechanisms, and software-based radiation mitigation strategies. Having designed, built, and integrated all subsystems, as well as performed multiple test campaigns at system and subsystem level, the team now aims at completing formal functional and environmental testing before undergoing the launch campaign, foreseen for 2022.

#### KEYWORDS ADS-B, CubeSat, low-power, miniaturization, telecommunications

# 1 | INTRODUCTION

At the 2015 World Radiocommunication Conference, the International Telecommunication Union (ITU) allowed for the use of the Automatic Dependent Surveillance-Broadcast (ADS-B) system in Earth-to-space applications, thereby extending the technology's use beyond line-of-sight communications with ground stations.<sup>1</sup> The discussion on the use of ADS-B beyond line-of-sight begun as early as 2008 at the German Aerospace Center,<sup>2,3</sup> with its advocates highlighting some limitations of the Automatic Dependent Surveillance - Contract (ADS-C) surveillance system which prevented continuous flight surveillance over non-radar airspaces. The loss of Malaysian Airlines Flight MH370 in 2014 triggered the discussion that accelerated the efforts to operationalize space-based ADS-B.

Several satellite missions have demonstrated the ADS-B detection technology in orbit. Following a first trial using high-altitude balloons,<sup>4</sup> the first space-based receiver was deployed as a secondary payload in the Proba-V mission,<sup>5,6</sup> relying on a 140-kg platform. The first commercial exploitation of this technology was deployed in the Iridium NEXT satellites,<sup>7</sup> which integrate a low Earth orbit (LEO) satellite constellation as

required in order to achieve real-time global coverage while respecting the ADS-B link budget.<sup>8</sup> Given their suitability for LEO orbits and their low-cost, CubeSat platforms have also become attractive for ADS-B deployment, as demonstrated by the GOMX-1,<sup>9</sup> GOMX-3,<sup>10</sup> and STU-2C<sup>11</sup> missions. These missions relied on 2 U and 3 U CubeSat platforms using a deployable helix antenna for ADS-B message decoding. Subsequent missions such as GOMX-4<sup>12</sup> and CANX-7<sup>13</sup> have relied on 6 U and 3 U platforms, respectively, and on patch rather than helix antenna configurations, thereby limiting the risk of deployment failure. All these missions relied on FPGA boards for signal decoding.

In this paper, we design a CubeSat mission aiming at further miniaturization and simplification of space-based ADS-B technology—the ISTSat-1. The ADS-B receiver is based on a general microprocessor rather than a dedicated FPGA board, allowing for lower power consumption which can be managed given the limited power generation capabilities of such a small platform (with the drawback of reduced computational power for decoding). While some ground-based receivers are also based on the dump1090 algorithm,<sup>14</sup> our proposal is implemented in a low-power ARM processor running a real time operating system rather than a full-fledged operating system for which the algorithm was originally designed. The ISTSat-1 spacecraft also features some innovations over traditional CubeSat platforms, such as the development of system-level software, which distributes functions over various subsystems rather than on a single central processor while efficiently sharing code, the use of redundant communications mechanisms and software-based radiation mitigation strategies, and an iterative and integrative development and testing process.<sup>15</sup> The mission design foresees the first use of a 1 U CubeSat platform for aircraft tracking.

The next section provides a high-level description of the mission, along with orbit analysis and space debris mitigation concerns. This is followed by a discussion of the system architecture and main design decisions. Sections 4–9 detail the design of the satellite's payload and supporting subsystems, namely, communications, power management, data handling, attitude determination and control, and structures. Finally, a description of the verification and validation efforts undergone so far is provided and the mission's main contributions and innovations are discussed.

# 2 | THE MISSION

ISTsat-1 builds upon the experience from previous missions and proposes a wide field-of-view (FOV), small form factor (patch) ADS-B antenna, installed on the nadir pointing face of the satellite. The scenario for the ADS-B link is depicted in Figure 1.

Aircraft typically use a blade antenna mounted on top of the fuselage and another at the bottom, alternating the transmission between the two antennas, using an RF carrier frequency of 1090 MHz. Its linearly polarized radiation pattern generally presents a null along the *z*-axis. This is responsible for a blind cone around the aircraft zenith. In practice, the null is commonly shaped by the influence of the aircraft fuselage and tail, as depicted in Figure 2.

Aircraft tracking data is collected in orbit, in a certain area and for a given time, and transmitted to the ground. It is then analyzed and correlated with ground-based tracking datasets to:

• Characterize the "Cone of Silence" when the satellite is at the aircraft antenna's zenith.



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FIGURE 2 Aircraft antenna radiation pattern: (A) ideal; (B) real

- Measure the performance parameters of the receiving chain,<sup>6</sup> namely,
  - Probability of target acquisition (PTA)-the likelihood that at least one position message from a certain aircraft is received
  - Probability of detection (POD)-the percentage of correctly decoded position messages
  - Probability of target identification (PTI)-the likelihood that at least one identification message from a certain aircraft is received
  - Probability of identification (POI)—the percentage of correctly decoded identification messages.

Two external ADS-B services (OpenSky Network and ADS-B Exchange) are used for accessing ground-based ADS-B information. The payload activity is scheduled such that messages are collected while the spacecraft passes above known ADS-B ground stations. Space-based data are then assessed against ground data in order to compute the previous metrics. Throughout the mission, different ADS-B ground stations will be used to understand how the metrics are influenced by factors such as latitude (which affects the pointing capabilities of the spacecraft) and air-craft density (which increases the likelihood of message collisions).

#### 2.1 | Mission analysis

The ISTSat-1 mission was developed under the support of ESA's Fly Your Satellite (FYS) program alongside other student missions such as LEDSat,<sup>16</sup> EIRSat-1,<sup>17</sup> and <sup>3</sup>CAT-4.<sup>18</sup>

The target orbit is determined by the FYS program, which means that it is an input to the design process rather than the output of an orbit selection analysis. Given that the S/C is foreseen to be launched from the ISS, the following orbit parameters were considered corresponding to the ISS orbit:

- Semi-major axis: 6791 km
- Eccentricity: 0.00137
- Inclination: 51.6°.

Mission design focused on understanding S/C visibility over the team's ground station in Oeiras, Portugal, and percentage of orbital period spent in eclipse. Additionally, the team was required to demonstrate compliance to space debris mitigation guidelines, namely, that atmospheric re-entry will occur in less than 25 years.

A visibility analysis was conducted using NASA's GMAT software.<sup>19</sup> The minimum elevation angle considered was 10°. Figure 3 presents the distribution of the number of daily passes over the ground station, as well as the distribution of the duration of the passes.

As seen in Figure 3, the satellite is visible on average four times per day, although some of the passages are of short duration. Nevertheless, the number of short duration passages is low and almost 30% of the passes have a duration of more than 5 min, ensuring data transfer possibilities virtually every day.

Another important metric for dimensioning the S/C, particularly the power subsystem, is the amount of time spent in eclipse in every orbit. Figure 4 shows that this time is always below 40% of the orbital period. This analysis also showed that the S/C is expected to be illuminated for long periods of time on some occasions, during which it might reach high temperatures. Under these circumstances, and because a cooling system was considered too complex, it may be necessary to partially shut off the S/C to prevent damage to the batteries.



FIGURE 3 Distribution of number of daily passes in a year



FIGURE 4 Percentage of time spent in eclipse over a year

Because there is no propulsion system, the S/C will re-enter in the Earth's atmosphere uncontrolled, decaying over time from the launch. ESA's DRAMA-OSCAR tool was used to assess the orbital lifetime. The analysis parameters were

- Initial date 2020-09-01 12:00:00.
- Reflectivity coefficient of 1.3.
- Solar & geomagnetic activity data from ESA.

Three scenarios were foreseen. The worst-case scenario (from a debris mitigation standpoint) corresponds to the maximum expected orbital lifetime. It assumes that the S/C's vertical axis is always aligned with the velocity vector, that is, that the front facing area is always that of a 10-cm

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# 3 | ISTSAT-1 SYSTEM OVERVIEW

The ISTsat-1 is composed of a flight platform, which ensures survivability in space, and a payload which consists of a compact ADS-B receiver and antenna. The global architecture is depicted in Figure 5.

The flight platform carries all the necessary technology to maximize the S/C mission lifetime and to provide the required logistics for the payload module. It includes the following functional subsystems: sensors, actuators, and algorithms for the attitude determination and control system (ADCS); On-board Data Handling (OBDH); Electrical Power Supply (EPS); communications processor and data storage (COM); modem, transceiver, and antennas for the Telemetry, Tracking and Communications (TTC) system.

The team decided to merge the ADCS and OBDH functional block into one physical subsystem, the On-Board Computer (OBC), since both functionalities could be properly handled by just one single processor. This subsystem is responsible for monitoring the other subsystems and resetting them should they be unresponsive. The MSP430F5438A microcontroller was chosen due to its good power to performance ratio and its space heritage.<sup>21</sup>

The TTC subsystem is responsible for maintaining the radio link with the ground segment (GS). It features a modem which handles the modulation function, transforming the digital data stream to be transmitted to the GS into a baseband analog stream that drives a transceiver and is delivered to the antenna. Conversely, it performs the demodulation of the incoming analog signals to a data stream to be delivered to other subsystems. It also features a Beacon module, a completely independent transmission system with its own modulator and power amplifier, which allows for tracking of the satellite in the case of failure of the main unit.

The EPS collects, stores, and distributes energy to the whole system. It features five solar panels for energy harvesting and a lithium-polymer battery. It implements a Maximum Power Point Tracking (MPPT) algorithm and an intelligent battery charger for power draw optimization but is also capable of directly delivering regulated power to the subsystems in case of microcontroller failure.

	Worst case	Nominal case	Best case
Cross-sectional area (m <sup>2</sup> )	0.010	0.015	0.0170
Dry mass (kg)	1.2	1.0	0.8
Drag coefficient	2.0	2.2	2.4
Expected lifetime (years)	1.8	1.22	0.86

# **TABLE 1** Values for the three scenarios



FIGURE 5 Global S/C architecture. The thick lines represent digital interfaces and the thin lines represent analog interfaces

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FIGURE 6 Exploded view of ISTSat-1

The COM subsystem, based on an ARM Cortex-M3 core, is responsible for the implementation of the communications protocol stack and is prepared to support computationally intensive protocols and data handling. It is the main data storage unit in the S/C, offering 16 MB of SRAM memory and 4 MB of FRAM memory. It also features a software radiation protection mechanism which detects faults in the memory banks and automatically shuts them off.

An exploded view of the ISTSat-1 subsystems is presented in Figure 6.

The ISTSat-1 establishes a radio link with the GS comprising one upstream and one downstream channel. These channels support the telemetry, command and control functionality, with payload data multiplexed on the downstream channel. This link is supported on a communications stack where Layer 2 is established on the AX.25 protocol, and the Layer 3 on the CubeSat Protocol (CSP). In addition, the beacon module conveys a synopsis of the satellite status, using Morse code.

The S/C features two main operating modes: safe mode and normal mode. Under safe mode, only the most basic functionalities are ensured. The payload and the COM subsystems are powered off, the OBC only executes communication and housekeeping tasks, and the TTC only employs the most robust (but slowest) modulation scheme for communications. This greatly limits the number of variables, which affects the system's behavior, allowing for easier debugging in case of an error and limiting the effect of software glitches. Upon deployment from the ISS, the S/C enters safe mode (after a 45-min delay, during which the detumbling algorithm decreases the rotation rate) so that the operations team can ensure that the basic functions are working correctly.

After the in-orbit commissioning is considered successful, a ground command is sent to switch to normal mode. Under this mode, all the subsystems are powered and the OBC performs ADCS tasks. The S/C is expected to be engaged in Normal Mode for most of its mission lifetime. safe mode can be automatically engaged following critical errors or low battery level and can only be disengaged following a ground command.

# 4 | ADS-B ANTENNA AND RECEIVER

Due to the nature of the mission, which does not feature constant ground station visibility for data downlink, the decoded messages are stored in the spacecraft and downloaded whenever there is a downlink opportunity.

The payload's function is to receive the ADS-B radiofrequency (RF) signals broadcast by commercial aircraft and translate them into messages, of which a digest is then downlinked to the GS. It includes a 1090-MHz patch antenna feeding the RF signal to the receiver placed in the -Z face of the satellite and pointing towards the nadir. It also features an ADS-B receiver, responsible for RF signal demodulation and decoding and for the interface with the remaining spacecraft subsystems, namely the OBC (for housekeeping) and the COM (for data storage).

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# TABLE 2 ADS-B link budget calculation

Budget calculation	Value	Unit	Rationale
(1) Transmit EIRP	27.0	dBW	500-W transmission power on aircraft
(2) Losses	-148.6	dB	(2.1) + (2.2)
(2.1) Free-space loss	-148.6	dB	For the maximum slant range of 590 km
(2.2) Atmospheric absorption	0.0	dB	From Table 2.2 in <sup>22</sup>
(3) Realized antenna gain	2.5	dBi	At nadir, as tested
(4) Received carrier power	-119.1	dBW	(1) – (2) + (3)
(5) Noise power	-139.7	dBW	(5.1) + (5.2) + (5.3)
(5.1) System noise temperature	24.1	dB K	Estimated 260-K noise temperature
(5.2) Boltzmann constant	-228.6	dB J/K	
(5.3) Bandwidth	64.8	dB Hz	For a 3-MHz bandwidth
(6) Carrier-to-noise ratio	20.2	dB	(4) – (5)





Preliminary requirements for the payload link budget were derived assuming a maximum altitude of 403.5 km, based on the ISS orbit, and a FOV of 90°, and are presented in Table 2.

The receiver can be further decomposed into two main sub-components: the RF front-end, responsible for the reception of the RF signal from the antenna and production of the base-band signal to be further processed; and the digital module, mainly composed of the multiple core microcontroller and responsible for the digitalization and sampling of the baseband signal, decoding ADS-B messages, and overall payload management.

#### 4.1 | Antenna

A circular polarized, non-deployable patch antenna was designed for installation at the bottom face of the satellite. This allows maintaining the link with aircraft, even if the CubeSat presents residual tumbling around the *z*-axis. It is based on the classical probe-fed square patch

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configuration with trimmed corners, using a single substrate layer. The feed point position determines mainly the antenna impedance, while the edge cuts determine the excitation of the orthogonal modes required for the generation of the circular polarization.

The antenna parameters—substrate permittivity, thickness, patch size, feed point, and trimmed corners—were selected or optimized for the best possible antenna performance under the influence of the CubeSat and of the VHF/UHF antennas for telemetry and telecommand. The antenna design was based on full wave simulations, and the RF tests were performed in anechoic chamber, mounted on a CubeSat mockup. The antenna was also tested outdoor, with an ADS-B receiver and ADS-B signals of actual flying planes up to 200-km distance.

Figure 7 represents the signal-to-noise ratio at the antenna port for different path lengths between the satellite and aircraft flying within a  $1600 \times 1600$  km area, centered on the CubeSat nadir. Each pixel represents the position of the aircraft, while its color represents the signal-to-noise ratio (SNR) according to the indicated scale. The aircraft transmitter power is 500 W, the CubeSat orbit altitude is 400 km, and the noise power at the antenna port is -105 dBm.

The final performance characteristics of the ADS-B patch antenna are summarized in Table 3.

#### 4.2 | Receiver

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Figure 8 shows the block diagram of the ADS-B receiver front-end which consists of a non-coherent power detector tuned at 1.09 GHz with a bandwidth of 2 MHz and a dynamic range of 40 dB. This bandwidth is enough to accommodate the estimated Doppler shift of about 27.25 kHz for an orbital velocity of 7.5 km/s at the expected orbital velocity.

#### TABLE 3 ADS-B antenna performance characteristics

Characteristic	Value	Units
Frequency	1090	MHz
Impedance	50	Ω
Bandwidth (VSWR < 2)	14	MHz
Polarization	LHCP	
Axial ratio ( $\theta$ < 30°)	<2.5	dB
CP directivity	4.3	dBi
Realized CP gain at nadir	2.5	dBi
Realized gain of the $E_{\theta}$ component	0.6	dBi
3-dB beam width	100	deg



FIGURE 8 ADS-B receiver RF front-end block diagram

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The receiver operates with input levels from -95 to -55 dBm. The front-end is divided in two sections: RF and baseband. The components used together with their main characteristics are also indicated in this figure.

The noise level referred at the antenna port is -106 dBm and the designed receiver sensitivity is -95 dBm. This is equivalent to a SNR of 11 dB which ensures a bit error rate (BER) of about  $10^{-4}$  for the PPM modulation used in ADS-B. At this input signal level, the power detector input should be about -45 dBm for proper operation, meaning that an overall receiver gain of about 50 dB is required. The LNA provides 30 dB of gain and another amplifier provides an additional 30 dB, totaling 60 dB. The extra 10 dB is required to compensate the insertion losses of the two SAW filters and the balun in the signal chain. The power detector outputs a baseband signal proportional to the RF power at its input (linear in dB). The signal bandwidth is then restricted to 2 MHz by means of a selective low pass filter. The resulting signal is then conditioned in gain and level to meet the range of the analog-to-digital converter (ADC) which digitizes the ADS-B signal. This converter has a 12-bit resolution and samples the signal at 12 Msample/s. It is embedded in the LPC4370 ARM microcontroller.

The digital part of the receiver (back-end) represents a significant departure from typical solutions which rely on FPGA implementations for decoding ADS-B signals (see, for instance, Ren et al.<sup>23</sup>). It is based on the ARM Cortex-M4 processor for embedded applications which includes an ARM Cortex-M0 coprocessor and an ARM Cortex M0 subsystem for managing peripherals, 282 kB of SRAM, advanced configurable peripherals, and multiple digital and analog peripherals, including a high-speed 12-bit ADC. The LPC4370 operates at CPU frequencies of up to 204 MHz.

The software architecture takes advantage of the multi-core architecture of the LPC4370 and of its high-speed ADC. The high-speed ADC is used for sampling the ADS-B baseband signal provided by the front-end, while the processors provide a parallel execution of different functions:

- ARM Cortex MO: signal acquisition. Buffering the ADC samples and performing the preamble detection of ADS-B messages.
- ARM Cortex M4: ADS-B messages reconstruction and decoding, error correction and filtering; handling of TC and collecting TM data; handling
  of housekeeping functions.
- ARM Cortex M0: overall receiver mode management and handling of the TM/TC interface with the OBC.

Figure 9 shows in detail all the functions required to handle the ADS-B messages up to the point to transfer the important ones to the S/C main storage unit in COM.

However, after an initial assessment of the performance of such functional distribution, one reached the conclusion that the first M0 core was too limited to sustain the desired ADC sampling rate (instead of the desired 12 Msa/s, only 3 Msa/s could be achieved). Fortunately, it was possible to work around the problem by using the LPC4370's DMAC to perform the transfer of samples between the fast ADC and a double buffer in memory.



FIGURE 9 ADS-B receiver back-end functional architecture

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It is from such buffer that, in parallel, the M4 performs the next required procedures in the receiver chain, namely, (i) low-pass filtering, (ii) phase alignment and preamble detection, (iii) message reconstruction and decoding, and (iv) filtering. The M4 core runs a specially adapted version of the dump1090 code<sup>14</sup> for decoding the ADS-B messages, which are then filtered out according to the area, time and other parameters defined in TC previously received from the Mission Control on Earth.

The filtered ADS-B messages are kept in a local storage that is used as a communication mechanism with the second M0 core. The messages are subsequently sent to the COM subsystem through the  $I^2C$  interface that is managed by this M0 core which is dedicated to this interfacing task.

#### 4.3 | Preliminary testing of the ADS-B receiver

In order to demonstrate the adequateness of the proposed receiver, a test setup was devised which allowed sending emulated ADS-B messages through the RF front-end at different rates.

### 4.3.1 | Test setup

A single ADS-B message, corresponding to an airborne position message, was encoded using a self-developed GNU-Radio script. This script was validated against the dump1090 algorithm. The GNU-Radio script includes a white noise generator to achieve the desired signal-to-noise ratio.

The signal was generated through a software-defined radio and fed into an attenuator such that signal power was similar to what is depicted in Table 2. Finally, the attenuator output was connected to the antenna socket in the ABS-B receiver.

In order to characterize the decoding performance under different conditions, messages were generated at rates of 1, 10, and 80 Hz, thus emulating passes over more or less crowded areas. The script was kept running for 100 s, after which the number of saved messages and detected preambles was recorded. For each rate, three different runs were recorded. The results represent an average of the three runs.

Power draw measurement was performed by a current sensor in the 3.3-V power supply. During each run, the current measurements were performed and recorded every 5 s. The results represent the average power draw over the run duration.

While this setup also allows testing the RF front-end, the major goals were to assess the decoding performance of the microprocessor, and to compare the overall receiver power draw an FPGA-based decoder.

#### 4.3.2 | Test results

The decoding performance of the proposed ADS-B receiver regarding correctly decoded messages and number of preambles detected can be seen in Table 4. The tests show that the receiver correctly decodes around 75% of messages sent at rates of up to 80 per second, which means that the spacecraft can detect around 60 aircraft each second. While this is fully compliant with mission objectives, which foresaw flying over remote areas with less than 20 aircraft, the fact that the decoding performance did not decrease significantly from 1 to 80 Hz suggests that message rate could be further increased. Unfortunately, at the time of writing, a software issue is causing a system crash at rates above 80 Hz, which prevented further testing.

The average power draw of the receiver was around 650 mW for all the runs. FPGA-based systems such as the receiver used for the GOMX-1 mission draw up to 1.3 W and decode up to 800 messages per second (as per datasheet found in GOMSpace<sup>24</sup>). The solution proposed in this paper, while not tested at this rate, allows decoding enough messages per second to identify up to 60 aircraft per second at a maximum power draw of 0.65 W.

Message rate (Hz)	Preambles detected (%)	Messages decoded (%)
1	96	77
10	96	75
80	95	74

**TABLE 4** Decoding efficiency under different aircraft density scenarios

# 5 | TELEMETRY, TRACKING, AND COMMUNICATION SYSTEM

The uplink, downlink and beacon main characteristics are summarized in Table 5.

In order to communicate with other subsystems, the TTC has three independent interfaces:

- UART (with OBC): provides a command interface and data in safe mode.
- SPI (with COM): provides the data in normal mode.
- I<sup>2</sup>C: S/C main bus which allows diagnostics and provides housekeeping data.

The private interfaces were chosen to be unaffected by disturbances in the main bus. Also, in case of an interface failure, the TTC can use the remaining interface to maintain the connection between the GS and the S/C.

In the normal mode, the OBC is responsible for controlling the TTC, selecting the modulation and the baud rate for the downlink. From that moment on, the TTC can communicate with the COM subsystem, which decodes the entire communication protocol stack, through the high-speed SPI interface. In safe mode, the communication is made exclusively through the OBC and the TTC with the RF link at the lowest rate: AFSK 1200. In this mode, the modem decodes the AX.25 messages to reduce the load on the OBC's CPU, which decodes the remainder of the communications protocol stack.

The TTC architecture is divided into four main blocks, as depicted in Figure 10: the transmitter, which amplifies the baseband signal to RF; the receiver, which amplifies and filters the RF signal to baseband; the modem, which modulates and demodulates the baseband signals and interfaces with the other subsystems; and the beacon, an autonomous system that broadcasts the S/C's most critical telemetry data.

#### TABLE 5 TTC main characteristics

Link	Modulation	Bit-rate	Bandwidth
Uplink 436.45 MHz	FM-AFSK	1200 bit/s	9.6 kHz
	BPSK	1200 bit/s	1.8 kHz
	BPSK	2400 bit/s	3.6 kHz
Downlink 145.895 MHz	FM-AFSK	1200 bit/s	9.6 kHz
	BPSK	4800 bit/s	14.4 kHz
	FSK (G3RUH)	9600 bit/s	19.2 kHz
	BPSK	9600 bit/s	14.4 kHz
	GMSK	9600 bit/s	19.2 kHz
	QPSK	19,200 bit/s	14.4 kHz
Beacon downlink 145.895 MHz	ASK CW (Morse)	20 WPM	250 Hz





**FIGURE 11** UHF receiver signal path

A power distribution system for these blocks was also developed, including current measuring and filtering to avoid disturbances in S/C's power system induced by the RF signals. All RF circuits are shielded inside metal cans. The hardware design considers the power constraints imposed by the EPS and the computational power of the baseband digital signal processor (modem).

#### 5.1 | UHF receiver

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The receiver is designed to operate with input signals as low as -105 dBm referred to the LNA input (1.26 µV @ 50 Ω). The front-end is a basic three-stage LNA tuned with a LC matching network, and out-of-band signals are attenuated somewhat by the antenna and the matching network. For increased resilience to out-of-band interference, a SAW filter precedes the final amplification stage prior to the mixer. The combined noise figure of the receiver is 1.1 dB. The mixer stage is a Gilbert Cell based mixer with 0-dB conversion gain, driven by a synthesizer, working 71-MHz above the carrier frequency (high-side conversion). Selectivity is provided by a SAW filter and IF amplification. The amplifier has differential outputs, suitable to drive the final quadrature mixer. This job is done by the mixer, which has a variable gain control, from 0 to 60 dB, referred to the mixer inputs. The whole assembly provides a combined receiver gain which can range from -26 to 120 dB, which is enough fulfill the sensitivity requirements proposed for the TTC front-end subsystem. Also, the input allows a discharge path to ground to avoid build up static charge. The signal path is depicted in Figure 11.

Automatic gain control (AGC) functions are implemented in three ICs and controlled by the digital signal processor (DSP) using two digital-to-analog converters (DAC): one DAC controls two LNAs (gain range from -80 to 30 dB) and another DAC controls the final mixer gain (0 to 60 dB). The two LNAs are located early on the receiver chain to prevent possible receiver saturation in the presence of a strong received signal. The mixer has a built-in IF power detector which is used to provide IF-RSSI information. This signal is sampled by a 10bit ADC and sent to the DSP. The AGC control algorithms are fully digital, implemented on the DSP using the IF-RSSI signal and the baseband I/Q signal energy. This allows for versatile control of AGC critical parameters, such as attack/decay times, AGC threshold and slope.

Using AFSK @ 1200 bit/s with a bandwidth of 3 kHz, the received signal level (sensitivity) required to achieve a BER =  $10^{-4}$  is -133 dBW (including 3 dB for receiving antenna pointing losses and 2 dB for implementation losses). In the receiver design an additional 2-dB margin was considered, so the receiver is designed with -135 dBW (-105 dBm) sensitivity.

#### 5.2 | VHF transmitter

The TTC transmitter is based on a full I/Q modulator. The baseband waveform is generated by the modem and fed into the quadrature modulator. The modulator output contains the passband signal, which is filtered by a SAW filter and goes into the driver and RF power amplifier. The transmitted power is controlled digitally by the DSP modem using a dual output DAC which controls the bias voltages of the power amplifier (PA). The signal path is depicted in Figure 12.

The DSP is responsible for the complete management of the TTC and is the only device communicating with other subsystems, namely, the COM and the OBC. Internal to the TTC, an interface named "modem interface" was defined. This interface consists of the signals connecting the modem to the TTC circuits.



FIGURE 12 Main VHF transmitter signal path

The transceiver is based around a low-power DSP and a low power stereo codec. This dual-MAC DSP can run with a clock frequency of up to 100 MHz with a power consumption of 0.26 mW/MHz. The codec provides 16-bit resolution with sampling frequencies up to 192 kHz.

Of the four main blocks, only the modem and beacon microcontrollers feature control software. These systems are independent and do not implement any operating system, that is, they are based on interrupt service routines (ISR) to meet the temporal requirements and on a main cycle that verifies if there are other actions to be taken, for instance, respond to other commands or other subsystems.

To minimize energy consumption, the DSP is normally in sleep mode, periodically checking for incoming radio signals through the RSSI value. The DSP is also "woken up" upon the reception of a message from any of the TTC interfaces (UART, SPI,  $I^2C$ ) to perform the requested action. Time critical tasks, modulation and demodulation, which are directly linked with the codec interface (I2S) run in their respective ISR. This ensures that  $I^2C$  communication is guaranteed even when the main loop is performing modulation and demodulation.

In safe mode, the DSP performs its normal function but in addition also performs the AX25 encoding/decoding. The housekeeping function is responsible for monitoring the TTC analog and digital chain (checking for errors/failures) and the interfaces with the remaining subsystems.

#### 5.3 | Beacon

The beacon transmitter is a separate and independent subsystem, apart from sharing the downlink antenna through an active RF switch. In case of general failure of the OBC, COM, DSP, or TTC transmitter, this switch is connected to the beacon's PA such that it can continue to broadcast telemetry data. This is assured by the arbitrator block. Both the transmitter parts of the modem and the beacon connect to this block with RTS/CTS signals. During normal operation, the TTC transmitter has priority and is granted access to the antenna. If the transmitter fails, antenna access is assigned to the beacon. Likewise, in case of a beacon failure, the access is assigned to the TTC transmitter.

The beacon power amplifier is keyed by a PIC16LF1718 microcontroller that also controls the beacon frequency synthesizer. The power amplifier has two bias inputs, one suitable for fine control of the output power by a DAC internal to the PIC and other for full on/off keying of

the transmitter. With this approach, it is possible to drive the power amplifier into Class C operation and thus achieve a higher efficiency than what is obtainable with the main transmitter PA, always off or operating in Class AB mode.

The microcontroller continuously measures the voltages given by the EPS along with other data relevant for telemetry downlink. After assembling the telemetry downlink frame, it encodes the data in Morse code and keys the transmitter PA bias inputs accordingly. The beacon can be powered either by the EPS or directly from the solar panel bus. This allows telemetry to be taken out of the S/C even if the EPS or the OBC fail.

# 6 | POWER MANAGEMENT

The EPS is the subsystem that provides the power to the satellite. It harvests the energy from the sun through the solar panels, stores it in Lithium-Polymer (LiPo) batteries and distributes and monitors power draw from each individual subsystem. Being a critical system in the S/C, it features redundant circuitry to ensure that power is available to other subsystems even if its microcontroller fails. It communicates with the OBC through the I<sup>2</sup>C interface, receiving commands and reporting its status for housekeeping purposes.

#### 6.1 | Hardware architecture

The ISTsat-1 electrical power subsystem uses five triple junction solar panels, a self-developed battery with four LiPo cells in a 2s2p configuration, an in-house designed controller, and a supervisor system. A charging port will be available to recharge the battery while the satellite is grounded. Figure 13 represents the overall architecture of the EPS.

The system voltage regulation is achieved in a two-stage process. In the first power processing stage, the input voltage coming from the solar panels is converted to an intermediate voltage using a MPPT algorithm. At this point, the voltage varies between 4 and 12 V depending on the energy produced by the solar panels. The second stage involves the output voltage regulators and current limiting systems that feed all the satel-lite subsystems.

A dedicated microprocessor is responsible for the EPS management. It controls and monitors current and voltage points within the EPS, handles communication with the OBC, controls the power lines that supply other sub-systems and, if necessary, engages redundant circuitry. The microcontroller also implements the MPPT algorithm. It also stores information regarding battery State of Charge and State of Health.

The proposed architecture allows for the power that is coming directly from the solar panels to be fed directly to the output voltage regulators through the power multiplexer, without involving the battery. The power on the energy supplying components (solar panels or charged battery) may not reach necessary the voltage at the output of the power multiplexer, lower than 6.2 V. Therefore, a SEPIC converter is used as a battery charger. If the voltage drops too much, it means that there is not enough energy being produced by the solar panels and so the batteries will not charge and instead will provide power to the rest of the system. After the multiplexer, the voltage should not go below 5 V, so buck



converters were implemented in the final regulation to achieve 3.3 and 5 V. The 3.3 V is the main voltage of the S/C system. The 5 V is only used to power the amplifiers in the TTC transmitter.

For redundancy purposes, the final 3.3 V regulator is doubled so that in case one should fail, the other should provide the power. In normal operation the power load between the final regulators is evenly distributed.

#### 6.2 | Battery

The battery is composed of four Varta LPP5037598HH Lithium Polymer cells. Each cell has a 5.2 Wh discharge capacity, nominal voltage of 3.7 V and a maximum discharge current of 2 A. These cells feature an embedded NTC temperature sensor and Protection Circuit Module (PCM) for protection against over discharge (below 3 V), over charge (over 4.32 V) and over current (over 2 A).

The battery configuration is a two series and two parallel cell connection (2s2p) generating 7.4 V nominal voltage and a discharge capacity of 20.8 Wh. The parallel arrangement allows for reducing the discharge load on each individual cell, improving longevity. The optimum charge current is about 600 mA. The battery uses a monolithic controller for charging in operational conditions. When the satellite is grounded, the battery can also be charged via the charging port. The charging port is connected directly to the battery terminals, so in this case, an external charger is required in order to meet the necessary charging profile of constant current and constant voltage modes.

Lithium-polymer cells can be permanently damaged if charged at temperatures below 0°C. However, as flight results for FITSAT-1 show,<sup>20</sup> negative temperatures can be expected for a 1 U CubeSat in an ISS orbit. In order to ensure survivability, the battery pack features a resistive heater which evenly dissipates heat to the cells. An adequate heat path is ensured by using electrically insulating, thermally conductive glue as an interface between the heater and the cells. The heater switches on when battery temperature falls below 1.5°C and off when the temperature goes above 6.5°C. The power of the heaters is controlled by a PWM signal and the maximum heat power is 510 mW.

#### 6.3 | Solar panels and MPPT

The solar panels used are triple junction InGaP/GaAs/Ge solar cells, with two cells connected in series in each panel. These panels can offer an efficiency of up to 29.5%. Each solar cell generates 2.665 V of open circuit voltage, and 0.544 A short circuit current, and the maximum power output is 2400 mW. The solar panels are, together with the VHF/UHF antenna, the only COTS components in the S/C.

To ensure that the maximum power is extracted, a MPPT is placed after the solar panels. This architecture employs three MPPT, and these are arranged with two opposing solar panels (+X, -X) per MPPT, except the +Z panel that is connected singularly to the MPPT. The other pairs are connected in parallel.

# 7 | DATA HANDLING

Two subsystems, the OBC and the COM, perform system data handling tasks.

#### 7.1 | On-board computer

The OBC is responsible for housekeeping tasks. It requests periodical diagnostics of other subsystems and detects and logs failures when they occur. The system has permanent storage capability, using a flash memory, and is responsible for maintaining the S/C time reference. It also gathers telemetry information from all subsystems, which is stored on both the OBC and COM while in normal mode and only on the OBC while in safe mode (during which the COM system is powered down).

The OBC is designed to be reliable and robust. In addition to the MCU internal watchdog, there is an external watchdog for redundancy, as well as a heartbeat signal between the EPS and the OBC. This cross-subsystem check offers fault detection, isolation, and recovery (FDIR) capability without the need for redundant units.

The subsystem relies on the MSP430F5438A Texas Instruments microcontroller. The hardware design features several modules, as depicted in Figure 14.

In a distributed processing system relying on an I<sup>2</sup>C bus, there is a concern that a single subsystem failure can inhibit the communications between all subsystems.<sup>25</sup> The protection of the communication bus between subsystems is done with an I<sup>2</sup>C buffer. This integrated circuit isolates the SDA and SCL lines of the main bus microcontroller and it can operate up to 400 kHz. It turns off automatically when any of the lines is











locked for more than 30 ms. After this period, the system attempts to recover the connection, forcing 16 pulses on the SCL line to unlock the  $l^2C$  interfaces that were locked.

# 7.1.1 | ADCS sensors

The OBC has two main sensors which are generate data for ADCS tasks. The first is an inertial measurement unit (IMU), which features a gyroscope, a magnetometer, and an accelerometer. This device has a user programmable gyroscope full-scale range of ±200/500/100/2000 dps, a user programmable accelerometer full-scale range of  $\pm 2/4/8/16 g$  and a magnetometer full-scale range of  $\pm 4800 \mu$ T. The second sensor is a 3-axis magnetic sensor featuring 8-user programmable scales and a full-scale range of  $\pm 810 \mu$ T.

Additionally, there are five sun sensors placed on each solar panel which have a signal conditioning circuit on the OBC board. These sensors have a reverse light current of 40 nA, a range of spectral bandwidth between 430 to 610 nm and an angle of sensitivity  $\pm 60^{\circ}$ .

#### 7.2 | Communications processor/data storage unit

The COM subsystem is responsible for handling the communications with the GS when the satellite is in "normal mode." However, when in "safe mode," the OBC module is the one that communicates with the GS, allowing the COM module to be idle, preserving energy.

Due to its computational capabilities and available memory, the COM subsystem receives and stores all payload data. Upon a downlink opportunity, it also compresses the data using the  $POCKET+^{26}$  algorithm which ensures an efficient use of the available bandwidth.

Besides storing mission data, COM module also stores housekeeping information from other subsystems, providing an interface for any system to log information about their operation. With this logging procedure, ground operators can enquire the satellite about any preceded errors, thus giving a chance to understand what might have caused them.

The COM hardware design is divided into several modules, as depicted in Figure 15.

Working as a central processing unit (CPU), the COM subsystem relies on an ARM Cortex-M3 based microcontroller, the LPC1833FET256 from NXP. Besides having an internal SRAM and Flash memories, external memories are also used, namely four 4-MB SRAM and eight 512-kB FRAM totaling 20 MB.

As a radiation protection measure, two current sensors are implemented, using an operational amplifier, measuring the current drawn by SRAM and FRAM memories, respectively. Attached to this implementation, six PMOS switches are connected to each pair of memory types to cut off their power if a high-current condition is detected. The COM uses I<sup>2</sup>C buffers which are connected to the main system I<sup>2</sup>C buses.



**FIGURE 16** System software architecture. The rectangles inside the OBC, COM, and PL subsystems represent different threads in FreeRTOS, while the ones in the EPS and TTC represent functions in the single main loop

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Besides having the internal watchdog from the microcontroller, an additional external watchdog timer working as voltage monitor is used in this subsystem.

#### 7.3 | System software

Each subsystem implements parts of different system-level functionalities. Some, such as energy harvesting and distribution or attitude determination and control, are relatively self-contained and mostly rely on information which is available within the subsystem. However, most of the ISTSat-1 functionalities (communications with the GS, ADS-B message storing, FDIR, etc.) rely on the exchange of information and execution of commands between subsystems. The system software architecture is depicted in Figure 16, with the main software blocks for each subsystem represented inside the dotted rectangles.

Four main modules are responsible for system-level interaction: ServiceI2C, ServiceHK, ServiceUART, and ServiceRadio.

The ServiceI2C module manages the physical and data link layers, handling redundancy in the two I<sup>2</sup>C lines and failed message retransmission. While all subsystems use a different microcontroller featuring a different I<sup>2</sup>C driver, they all share a common API (i.e., hardware abstraction layer), enabling the reuse of code.

The ServiceUART and ServiceRadio modules handle the radio link communication protocol stack. The TTC acts as a modem, converting digital bit streams into analog signals and vice-versa. The separation of the two services is due to the different processing of the protocol stack for Safe and Normal Mode. The ServiceUART module manages radio communications in Safe Mode, with the TTC handling the AX.25 protocol and the OBC the CSP and RDP protocols. Additionally, it also deals with some commands between the OBC and TTC. The ServiceRadio module handles radio communications in normal mode, with the COM being responsible for AX.25, CSP and RDP protocols, freeing the TTC DSP to cope with higher bitrate modulation schemes.

The ServiceHK (housekeeping) module manages the application-level protocol. Specifically, it is responsible for receiving, decoding, interpreting, and handling messages between subsystems, which can be data requests or command execution requests. For example, the EPS may receive a command execution request from the OBC to cut power to the ADS-B payload (which happens when transitioning from normal to safe mode). This message is decoded and validated by the ServiceHK module in the EPS, which then executes the command as part of a subsystemspecific task. The ServiceHK module is called again to encode the results of the execution into a message which is sent to the OBC, which logs the message for downlink.

The additional work involved in the virtualization of application-level software used for internal communications has brought clear benefits to overall system development process. Even though each subsystem has its own set of data variables, reports, commands, configuration parameters and events, the infrastructure of the housekeeping service is the same for all, which made it very simple to add or remove functionality without major rework of logical interfaces between subsystems.

Another benefit of separating communication interfaces from the functional application-level management is that any correctly encoded message in the I<sup>2</sup>C bus can be interpreted by a subsystem, regardless of how and where from it was sent. This was useful for development as a GS command, typically sent through the radio link, could be sent through an Electrical Ground Support Equipment (EGSE) directly accessing the I<sup>2</sup>C bus without changing the logical implementation.

# 8 | ATTITUDE DETERMINATION AND CONTROL SYSTEM

The ADCS has two main objectives: to reduce the angular momentum of the satellite after deployment and to point the S/C to nadir. This is achieved through three different functions, namely, the determination of current attitude, the calculation of the required correction, and the actuation for correction. For attitude determination, three types of sensors are used: magnetometer, gyroscope, and sun sensors. The determination algorithm uses the sensor data to compute the state vector of the satellite. The control algorithm generates command values for the actuators. Three perpendicular magnetorquers, enclosed within the -X, -Y, and +Z solar panels, are used as actuators for attitude control.

# 8.1 | Coordinate systems

The S/C uses three coordinate systems depending on the purpose computation purpose.

The Earth-centered inertial (ECI) frame is defined with the z-axis normal to Earth's orbital plane, the x-axis pointing to vernal equinox and the y-axis perpendicular to both. It is used to represent the S/C position and the evolution of Earth relative to the Sun's position, which allows the use of sun sensors.

The Earth-centered Earth fixed (ECEF) is defined with the *z*-axis aligned with true north and the *x*-axis in the equatorial plane and prime meridian. This is used to compute Earth magnetic field S/C and predict GS contact.

The body fixed (BF) frame is defined with the z-axis normal to the top and bottom faces of the S/C, the x-axis normal to the face with the access port and the y-axis defined to form a proper orthonormal frame. This system is used to represent the sensors readings and actuators inputs and later, combined with the ECI, to determine the S/C's attitude.

# 8.2 | Determination algorithm

There are numerous algorithms already used and usually involve classical filtering methods, using Kalman filters, extended Kalman filters or complementary filters. These data fusion algorithms can be quite complex and require a large computational load. The team's approach is based on an alternative algorithm which is less computationally intensive and is detailed in Mahony et al.<sup>27</sup>

This algorithm is based on the correction of the rotation rate provided by the gyro. The correction is made by integrating the estimated rotation rate with an error vector. Meanwhile, this correction vector is provided by a proportional integral (PI) controller, considering the system's attitude, which is determined using other means. In this case, the combination of magnetic and sun vector is used to determine the exact position of the system's attitude at the time the measurement is made.

The sun vector, magnetic field, and the angular velocity are measured every iteration. The normalization of the magnetic and gravitational fields is then performed, since only their direction is needed. Then, the vector error is calculated, and the PI controller is applied to correct the rotation rate. Finally, the rate of rotation is corrected and integrated, in order to calculate the angular velocity. Based on this information, a rotation quaternion can be generated to calculate the satellite's current attitude quaternion representation.

The reference vectors at each instant of time are generated based upon the satellite's position. For this to be possible, the satellite needs to know its own position either by receiving data with its position over the time or through estimation. The latter is the better choice if low position accuracy is needed, because the former takes up data bandwidth. This is the case for ISTSat-1, as the magnetic field vector and sun reference vector computation errors due to position error are very small. One issue with this method is the error accumulates over time, which means that two-line element information must be updated at every GS pass.

# 8.3 | Control algorithm

With regard to detumbling, or the reduction of angular momentum after deployment, the Bdot algorithm was chosen. It calculates the angular rate through magnetic field variations and creates a torque in the opposing direction.

The pointing controller, which is deployed only when angular rate is below  $2^{\circ}$ /s, points the *z*-axis of the S/C to a desired point through the misalignment between the pointing vector and the *-z*-axis. The input error of the alignment between axes is computed through a simple cross product between the two vectors, both written in the body frame representing a rotation of the body frame. Then the error is fed to a proportional derivative controller which computes the pointing torque.

#### 8.4 | Actuators

Only one type of actuator was considered, namely, the magnetorquer. Three magnetorquers are placed on the back of three solar panel PCBs in the -X, -Y, and +Z faces. These devices are specific coils that when charged with electric current produce a magnetic dipole that will interact with the Earth magnetic field, generating an aligning torque. Given the torque requirements, the duty cycle of the output signal as function of the desired torque can be obtained. For safety reasons, a limit of 0.8 was imposed in the output of the actuator controller to avoid duty cycles higher than 80% to avoid the continuous magnetic disturbances it could cause to other systems also consequently save energy. Likewise, a minimum duty-cycle of 10 kHz was also imposed to make sure the PWM drivers do not get near their frequency limits.

#### 9 | STRUCTURAL DESIGN

Although the mechanical design for a 1 U CubeSat can be considered simple, it is critical for mission success. Mechanical failures can also jeopardize other CubeSat missions or even launch vehicles. Because of this, the focus during the structural design phase was mostly on demonstrating requirement compliance through analysis. The ISTSat-1 structure is a six-part assembly. Each part is individually machined out of 7075-T6 aluminum alloy. There are two types of parts: the sideframes and the arm links. The structure is shown in Figure 17.

Three types of structural analyses were performed using the finite elements method: linear static, modal, and random vibration. The goal of the first was to demonstrate the capability to withstand the maximum quasi-static acceleration imposed by the launch vehicle. The goal of the last two is to demonstrate the capability to withstand vibration loads, particularly in the first moments after launch when acoustic noise from the



#### FIGURE 17 ISTSat-1 structure

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TABLE 6	Random	vibration	analysis	ASD	profile
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Frequency (Hz)	ASD (g <sup>2</sup> /Hz)
20	0.057
153	0.057
190	0.099
250	0.099
750	0.055
2000	0.018
OA (grms)	9.47





FIGURE 19 ISTSat-1 development model (left) and proto-flight model (right)

engines is reflected off the ground. All analyses were performed for three sets of boundary conditions assuming that the X, Y, or Z axis will be aligned with the launcher velocity vector.

For the static analysis, an overall acceleration of 19 g was applied to the model. Maximum displacement occurred in the EPS, which was expected as it is the heaviest board. The minimum margin of safety, for a 1.5 safety factor, was 3.8 for yield strength, and 5.5 for ultimate tensile strength.

The modal analysis showed that the first fundamental frequency is approximately 190 Hz, which is well above 100 Hz as required by the Japan Aerospace Exploration Agency.<sup>28</sup>

The random vibration analysis was run using the input Acceleration Spectral Density (ASD) shown in Table 6. Structural dampening was set at 3%.

The analysis resulted in a minimum margin of safety of 2.3 for a factor of safety of 1.5. This result was calculated with 3 $\sigma$  significance.

# 10 | SYSTEM VERIFICATION

As of June 2021, the design of the ISTSat-1 spacecraft and the supporting ground station is finished, and flight hardware has been produced. The flight systems are currently integrated in a flatsat configuration (as shown in Figure 18). This configuration allows for continuous integration testing as the functionalities are perfected.

Along with integration testing, the team has had the opportunity of performing multiple environmental test campaigns, including an ionizing radiation test which demonstrated the software-based radiation mitigation strategy for the OBC, a non-ionizing radiation (electromagnetic compatibility) test which demonstrated the immunity of the EPS, OBC and COM subsystems against disturbing electromagnetic radiation and also the S/C's compliance to emitted radiation standards, a full vibration and thermal-vacuum test campaign for battery qualification,<sup>15</sup> and a thermal test determining the resilience of the TTC to extreme temperature variations.

The next steps towards the launch preparation campaign include the formal full functional and mission testing campaign, under which the team will demonstrate compliance to ISS and program requirements as well as to its own mission requirements. These tests will be performed on the proto-flight model, shown in Figure 19. After this, an environmental test campaign will demonstrate the adequateness of the design in withstanding the expected vibration profile during launch and the operation in extreme temperatures under vacuum conditions.

# 11 | CONCLUSION

The ISTSat-1 spacecraft design has shown that further miniaturization of space-based aircraft tracking technology is possible. The ADS-B receiver and patch antenna perform message decoding and filtering in a compact format, with no deployable antenna mechanisms, and with very power consumption using a general-purpose microprocessor. The proposed design represents the smallest ADS-B payload to be developed for a CubeSat mission. The in-house development of all the major subsystems lead to the creation of innovative solutions which differ from what is commercially available from CubeSat module suppliers. The EPS allows for safe power supply even in the case of microcontroller failure. Because it was developed holistically and not through the merging of separate subsystems, the entire on-board data handling system allows for multiple levels of redundancy, including software-based radiation effects mitigation. Telemetry transmission is also redundant. These features increase confidence in the success of the overall mission.

The development process itself was innovative, with multiple subsystem prototypes undergoing early system integration testing, allowing for system software development to be developed and tested early in the process. In-house development made "tinkering" with prototypes easy, which would not have been possible if the subsystems were purchased at "space-grade" prices.

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#### DATA AVAILABILITY STATEMENT

The test data and scripts used in the preparation of the article can be accessed in the online public repository (https://gitlab.com/joaoplmonteiro/ ijscn-data).

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