

Digital Light Processing™ for High-Brightness, High-Resolution Applications

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ABSTRACT

Electronic projection display technology for high-brightness applications had its origins in the Gretag Eidophor, an oil film-based projection system developed in the early 1940s. A number of solid state technologies have challenged the Eidophor, including CRT-addressed LCD light valves and active-matrix-addressed LCD panels. More recently, in response to various limitations of the LCD technologies, high-brightness systems have been developed based on Digital Light Processing™ technology. At the heart of the DLP™ projection display is the Digital Micromirror Device™ (DMD™), a semiconductor-based array of fast, reflective digital light switches that precisely control a light source using a binary pulsewidth modulation technique.

This paper describes the design, operation, performance, and advantages of DLP-based projection systems for high-brightness, high-resolution applications. It also presents the current status of high-brightness products that will soon be on the market.

Key Words: Digital Micromirror Device, DMD, Digital Light Processing, DLP, spatial light modulator, SLM, microelectromechanical systems, MEMS, digital imaging, projection displays.

1.0 INTRODUCTION

Large-screen, high-brightness electronic projection displays serve four broad areas of application: (1) Electronic presentations (e.g., business, education, advertising), (2) entertainment (e.g., home theater, sports bars, theme parks, electronic cinema), (3) status and information (e.g., military, utilities, transportation, public, sports) and (4) simulation (e.g., training, games). The electronic presentation market is being driven by the pervasiveness of software that has put sophisticated presentation techniques (including multimedia) into the hands of the average PC user.

A survey of high-brightness (>1000 lumens) electronic projection displays is shown in *Figure 1*. The brightness (lumens) is plotted against the brightness efficiency (lumens/watt). Three types of projection display technologies are compared in Figure 1, oil film, CRT-LCD, and AM-LCD. Developed in the early 1940s at the Swiss Federal Institute of Technology

and later at Gretag AG, oil film projectors (including the GE Talaria) have been the workhorse for applications that require projection displays of the highest brightness [1]. But the oil film projector has a number of limitations including size, weight, power, setup time, stability, and maintenance. In response to these limitations, LCD-based technologies have challenged the oil film projector. These LCD-based projectors are of two general types: (1) CRT-addressed LCD light valves and (2) active-matrix (AM) LCD panels.

LCD-based projectors have not provided the perfect solution for the entire range of high-brightness applications. CRT-addressed LCD light valves have setup time and stability limitations. Most active-matrix LCDs used for high-brightness applications are transmissive and, because of this, heat generated by light absorption cannot be dissipated with a heatsink attached to the substrate. This limitation is mitigated by the use of large-area LCD panels with forced-air cooling. However, it may still be difficult to implement effective cooling at the highest brightness levels.

In response to these and other limitations, as well as to provide superior image quality under the most demanding

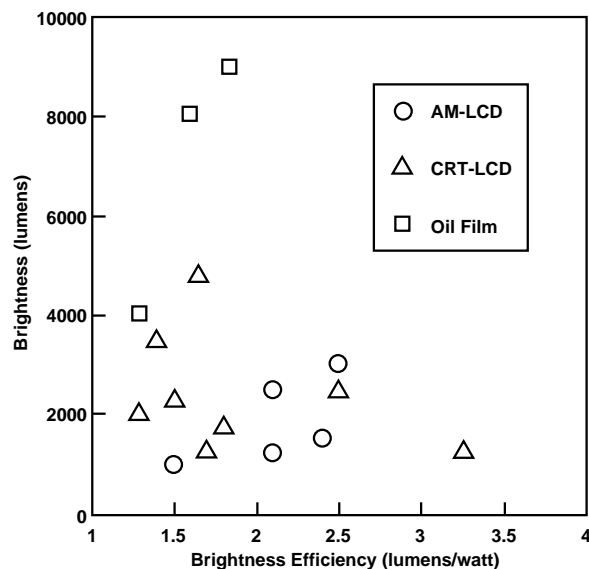


Figure 1. Survey of high-brightness projection displays

environmental conditions, high-brightness projection display systems have been developed based on Digital Light Processing™ technology. DLP™ is based on a microelectromechanical system (MEMS) device known as the Digital Micromirror Device™ (DMD™). The DMD, invented in 1987 at Texas Instruments, is a semiconductor-based array of fast, reflective digital light switches that precisely control a light source using a binary pulsewidth modulation technique. It can be combined with image processing, memory, a light source, and optics to form a DLP system (Figure 2) capable of projecting large, bright, seamless, high-contrast color images. Figure 3 shows a DLP projector in an

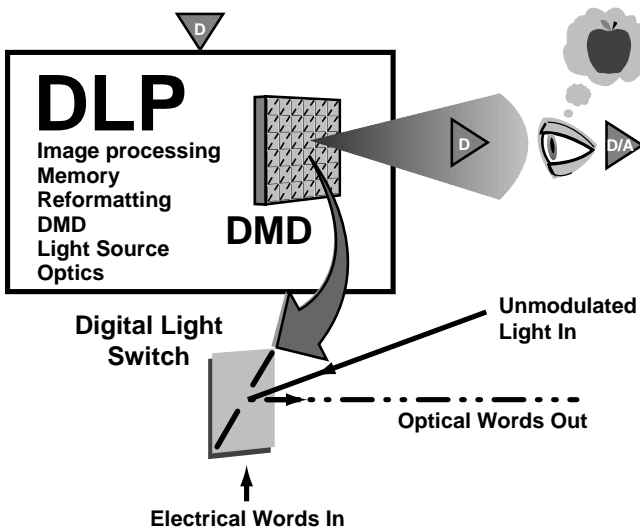


Figure 2. Digital Light Processing system



Figure 3. DLP projector in auditorium environment

auditorium environment. This photo was taken at the Texas Instruments Digital Imaging Business Center in Dallas, Texas.

DLP-based projection displays are well-suited to high-brightness and high-resolution applications: (a) the digital light switch is reflective and has a high fill factor, resulting in high optical efficiency at the pixel level and low pixelation effects in the projected image; (b) as the resolution and size of the DMD increase, the overall system optical efficiency grows because of higher lamp-coupling efficiency; (c) because the DMD operates with conventional CMOS voltage levels (~5 volts), integrated row and column drivers are readily employed to minimize the complexity and cost impact of scaling to higher resolutions; (d) because the DMD is a reflective technology, the DMD chip can be effectively cooled through the chip substrate, thus facilitating the use of high-power projection lamps without thermal degradation of the DMD; and (e) finally, DLP-based systems are all-digital (digital video in, digital light out), so reproduction of the original video source material is accurate and the image quality is stable with time [2].

The general movement of the display industry is in the digital direction. Digital sources that are currently available include digital video disk (DVD), digital satellite system (DSS), and the Internet (World Wide Web). In the future, the recently approved Advanced Television Standard (ATV) and the digital distribution of movies (digital cinema) will be added to the list of digital sources. Interfacing these digital sources to currently available analog displays requires digital-to-analog conversion and, in some instances, analog encoding (e.g., s-video or composite), which result in degradation of the source image quality. DLP-based displays, on the other hand, preserve the digital integrity of the source image all the way to the eye. The result is the best possible video quality.

A comprehensive, chronological list of DLP and DMD publications and presentations [2-59] is presented in Section 8.0. The list includes general DLP review papers and papers on early DMD development, system electronics, optics, DMD mechanical modeling, manufacturing, and reliability. It also includes references to DMD-based digital printing technology [4,24,37,56].

2.0 DMD LIGHT SWITCH

2.1 The mirror as a switch

The DMD light switch (Figure 4) is a member of a class of devices known as microelectromechanical systems. Other MEMS devices include pressure sensors, accelerometers, and microactuators. The DMD is monolithically fabricated by CMOS-like processes over a CMOS memory. Each light switch has an aluminum mirror, 16 μm square, that can reflect light in one of two directions, depending on the state of the underlying memory cell. Rotation of the mirror is accomplished through electrostatic attraction produced by

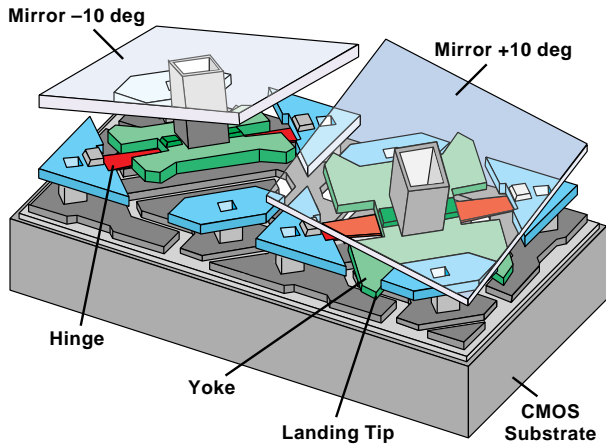


Figure 4. Two DMD pixels (mirrors are shown as transparent)

voltage differences developed between the mirror and the underlying memory cell. With the memory cell in the on (1) state, the mirror rotates to +10 degrees. With the memory cell in the off (0) state, the mirror rotates to -10 degrees. A closeup of DMD mirrors operating in a scanning electron microscope (SEM) is shown in *Figure 5*.

By combining the DMD with a suitable light source and projection optics (*Figure 6*), the mirror reflects incident light either into or out of the pupil of the projection lens by a simple beam-steering technique. Thus, the (1) state of the mirror appears bright and the (0) state of the mirror appears dark. Compared to diffraction-based light switches, the beam-steering action of the DMD light switch provides a superior tradeoff between contrast ratio and the overall brightness efficiency of the system.

2.2 Grayscale and color operation

Grayscale is achieved by binary pulsewidth modulation of the incident light. Color is achieved by using color filters, either stationary or rotating, in combination with one, two, or three DMD chips (*Section 3.2*).

The DMD light switch is able to turn light on and off rapidly by the beam-steering action of the mirror. As the mirror rotates, it either reflects light into or out of the pupil of the projection lens, to create a burst of digital light pulses that the eye interprets as an analog image (*Figure 2*). The optical switching time for the DMD light switch is $\sim 2 \mu\text{s}$. The mechanical switching time, including the time for the mirror to settle and latch, is $\sim 15 \mu\text{s}$ [36].

The technique for producing the sensation of grayscale to the observer's eye is called binary pulsewidth modulation. The DMD accepts electrical words representing gray levels of brightness at its input and outputs optical words, which are interpreted by the eye of the observer as analog brightness levels.

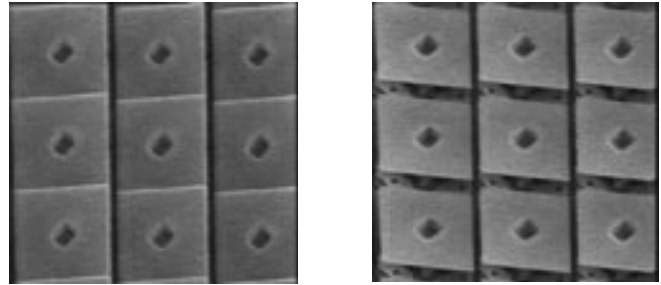


Figure 5. SEM video images of operating DMD

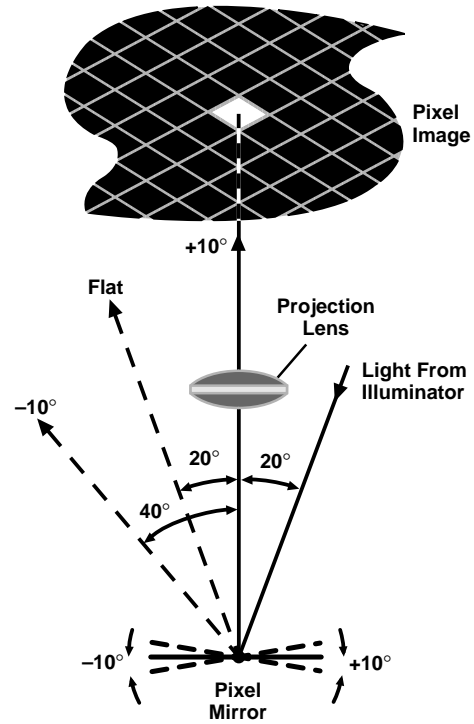


Figure 6. DMD optical switching principle

The details of the binary pulsewidth modulation (PWM) technique are illustrated in *Figure 7*. For simplicity, the PWM technique is illustrated for a 4-bit word (2^4 or 16 gray levels). Each bit in the word represents a time duration for light to be on or off (1 or 0). The time durations have relative values of $2^0, 2^1, 2^2, 2^3$, or 1, 2, 4, 8. The shortest interval (1) is called the least significant bit (LSB). The longest interval (8) is called the most significant bit (MSB). The video field time is divided into four time durations of $1/15, 2/15, 4/15$, and $8/15$ of the video field time. The possible gray levels produced by all combinations of bits in the 4-bit word are 2^4 or 16 equally spaced gray levels (0, $1/15, 2/15 \dots 15/15$). Current DLP systems are either 24-bit color (8 bits or 256 gray levels per primary color) or 30-bit color (10 bits or 1024 gray levels per primary color).

In the simple example shown in *Figure 7*, spatial and temporal artifacts can be produced because of imperfect integration

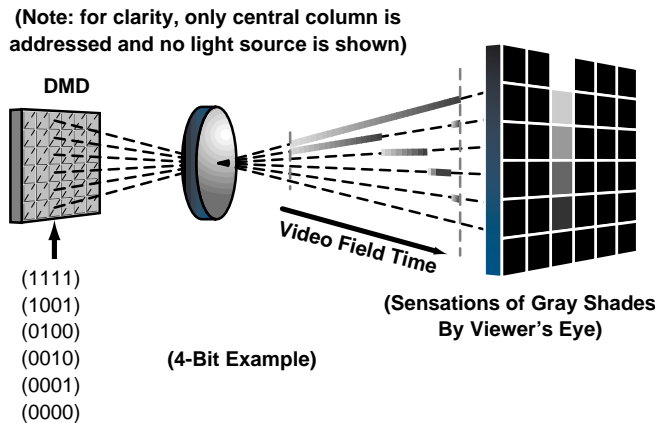


Figure 7. DMD binary pulsewidth modulation (4-bit example)

of the pulsed light by the viewer's eye. These artifacts can be reduced to negligible levels by a "bit-splitting" technique [26]. In this technique, the longer duration bits are subdivided into shorter durations, and these split bits are distributed throughout the video field time. DLP displays combine pulsewidth modulation and bit-splitting to produce a "true-analog" sensation, but with greater accuracy and stability than can be achieved by analog projection systems.

2.3 DMD cell architecture and fabrication

The DMD pixel is a monolithically integrated MEMS superstructure cell fabricated over a CMOS SRAM cell (Figure 8) [51]. An organic sacrificial layer is removed by plasma etching to produce air gaps between the metal layers of the superstructure. The air gaps free the structure to rotate about two compliant torsion hinges. The mirror is rigidly connected to an underlying yoke. The yoke, in turn, is connected by two thin, mechanically compliant torsion hinges to support posts that are attached to the underlying substrate.

The address electrodes for the mirror and yoke are connected to the complementary sides of the underlying SRAM cell. The yoke and mirror are connected to a bias bus fabricated at the metal-3 layer. The bias bus interconnects the yoke and mirrors of each pixel to a bond pad at the chip perimeter [36]. An off-chip driver supplies the bias waveform necessary for proper digital operation (Section 2.4). The DMD mirrors are 16 μm square and made of aluminum for maximum reflectivity. They are arrayed on 17 μm centers to form a matrix having a high fill factor ($\sim 90\%$). The high fill factor produces high efficiency for light use at the pixel level and a seamless (pixelation-free) projected image.

Electrostatic fields are developed between the mirror and its address electrode and the yoke and its address electrode, creating an efficient electrostatic torque. This torque works against the restoring torque of the hinges to produce mirror

and yoke rotation in the positive or negative direction. The mirror and yoke rotate until the yoke comes to rest (or lands) against mechanical stops that are at the same potential as the yoke. Because geometry determines the rotation angle, as opposed to a balance of electrostatic torques employed in earlier analog devices, the rotation angle is precisely determined.

The fabrication of the DMD superstructure begins with a completed CMOS memory circuit. A thick oxide is deposited over metal-2 of the CMOS and then planarized using a chemical mechanical polish (CMP) technique. The CMP step provides a completely flat substrate for DMD superstructure fabrication, ensuring that the projector's brightness uniformity and contrast ratio are not degraded.

Through the use of six photomask layers, the superstructure is formed with layers of aluminum for the address electrode (metal-3), hinge, yoke and mirror layers and hardened photoresist for the sacrificial layers (spacer-1 and spacer-2) that form the two air gaps. The aluminum is sputter-deposited and plasma-etched using plasma-deposited SiO_2 as the etch mask. Later in the packaging flow, the sacrificial layers are plasma-ashed to form the air gaps.

The packaging flow begins with the wafers partially sawed along the chip scribe lines to a depth that will allow the chips to be easily broken apart later. The partially sawed and cleaned

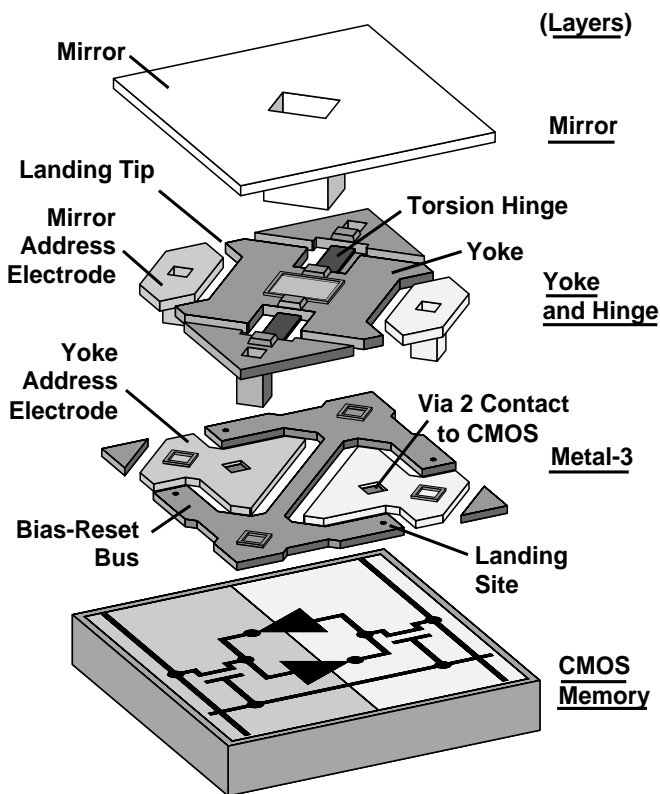


Figure 8. DMD pixel exploded view

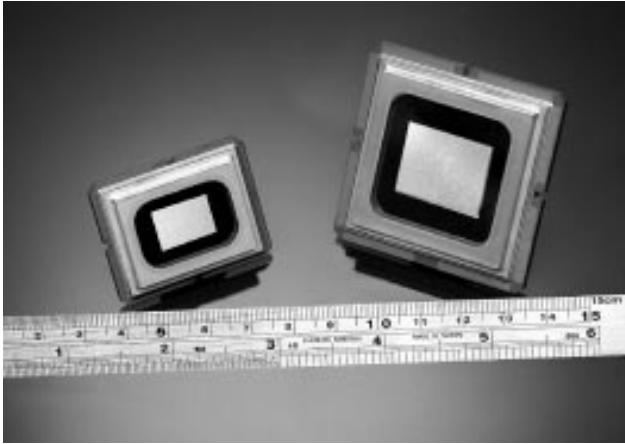


Figure 9. Packaged DMD chips

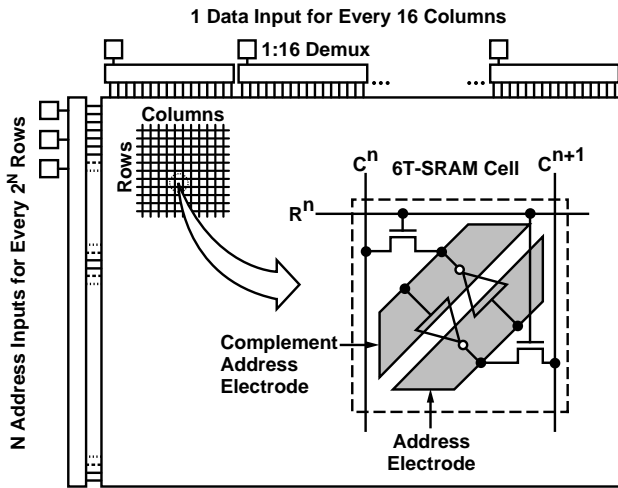


Figure 10. Organization of the DMD chip

wafers then proceed to a plasma etcher that is used to selectively strip the organic sacrificial layers from under the DMD mirror, yoke, and hinges. Following this process, a thin lubrication layer is deposited to prevent the landing tips of the yoke from adhering to the landing pads during operation. Before separating the chips from one another, each chip is tested for full electrical and optical functionality by a high-speed automated wafer tester [55]. Finally, the chips are separated from the wafer, plasma-cleaned, relubricated, and hermetically sealed in a package. Further manufacturing details are contained in references [36, 43, 51, 52, 57].

Figure 9 shows packaged DMD chips in two array sizes, SVGA (800 × 600) and SXGA (1280 × 1024). The diagonals of the active area, as discussed in Section 4.1, are 0.7 in. (SVGA) and 1.1 in. (SXGA).

2.4 Electronic operation

The DMD pixel is inherently digital because of the way it is electronically driven [5]. It is operated in an electrostatically

bistable mode by the application of a bias voltage to the mirror to minimize the address voltage requirements. Thus, large rotation angles can be achieved with a conventional 5-volt CMOS address circuit.

The organization of the DMD chip is shown in Figure 10. Underlying each DMD mirror and mechanical superstructure cell is a six-transistor SRAM. Multiple data inputs and demultiplexers (1:16) are provided to match the frequency capability of the on-chip CMOS with the required video data rates. The pulsewidth modulation scheme for the DMD requires that the video field time be divided into binary time intervals or bit times. During each bit time, while the mirrors of the array are modulating light, the underlying memory array is refreshed or updated for the next bit time. Once the memory array has been updated, all the mirrors in the array are released simultaneously and allowed to move to their new address states.

This simultaneous update of all mirrors, when coupled with the PWM bit-splitting algorithm described in Section 2.2, produces an inherently low-flicker display. Flicker is the visual artifact that can be produced in CRTs as a result of brightness decay with time of the phosphor.

Because CRTs are refreshed in an interlaced scan-line format, there is both a line-to-line temporal phase shift in brightness as well as an overall decay in brightness. DLP-based displays have inherently low flicker because all pixels are updated at the same time (there is no line-to-line temporal phase shift) and because the PWM bit-splitting algorithm produces short-duration light pulses that are uniformly distributed throughout the video field time (no temporal decay in brightness).

Proper operation of the DMD is achieved by using the bias and address sequence shown in Figure 11 and detailed in Table 1.

The bias voltage has three functions. First, it produces a bistable condition to minimize the address voltage require-

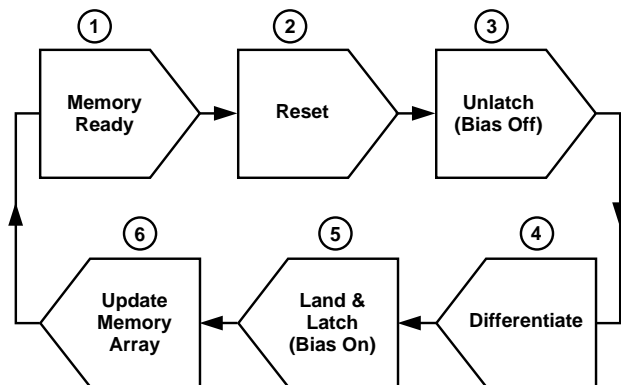


Figure 11. DMD address and reset sequence

ment, as previously mentioned. In this manner, large rotation angles can be achieved with conventional 5-volt CMOS. Second, it electromechanically latches the mirrors so that they cannot respond to changes in the address voltage until the mirrors are reset. The third function of the bias is to reset the pixels so that they can reliably break free of surface adhesive forces and begin to rotate to their new address states.

Although the metal surfaces of the superstructure are coated with a passivation layer or lubrication layer, the remaining van der Waal or surface forces between molecules require more than the hinge-restoring force to reliably reset the mirrors. A reset voltage pulse applied to the mirror and yoke causes the spring tips of the yoke (*Figure 12*) to flex. As the spring tips unflex, they produce a reaction force that causes the yoke landing tips to accelerate away from the landing pads, producing a reliable release from the surface [52].

2.5 DMD reliability

Steady improvements in DMD reliability have been made [28, 49, 52]. Some of these are listed below:

- A “bipolar reset” address scheme that leads to greater dynamic address margin.
- An improved hinge material that reduces metal creep that can occur under high-duty-factor and high-temperature operating conditions.

Table 1. DMD address and reset sequence

<ol style="list-style-type: none"> 1. <u>Memory ready</u>—All memory cells under the DMD have been loaded with the new address states for the mirrors. 2. <u>Reset</u>—All mirrors are reset in parallel (voltage pulse applied to bias bus). 3. <u>Unlatch</u>—The bias is turned off to unlatch mirrors and allow them to release and begin to rotate to flat state. 4. <u>Differentiate</u>—Retarding fields are applied to the yoke and mirrors in order to rotationally separate the mirrors that remain in the same state from those that are to cross over to a new state. 5. <u>Land and latch</u>—The bias is turned on to capture the rotationally separated mirrors and enable them to rotate to the addressed states, then settle and latch. 6. <u>Update memory array</u> (one line at a time)—The bias remains turned on to keep the mirrors latched so as to prevent them from responding to changes in the memory, while the memory is written with new video data. 7. <u>Repeat sequence</u> beginning at step 1.

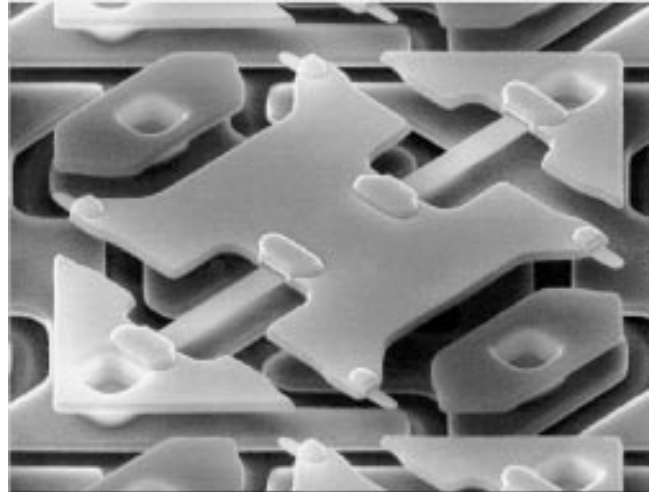


Figure 12. SEM photomicrograph of yoke and spring tips (mirror removed)

- Improved packaging techniques that preserve the “lubricity” of the landing surface over a wide range of environmental conditions.
- A new architecture that incorporates spring tips at the landing tip of the yoke. The result is greater operating margins as the yoke releases (resets) from the underlying surface.
- A particle reduction program that has dramatically reduced particle contamination within the DMD package.

The DMD has passed a series of tests to simulate actual DMD environmental operating conditions, including thermal shock, temperature cycling, moisture resistance, mechanical shock, vibration, and acceleration testing and has passed all of these tests. In addition to these, other tests have been conducted to determine the long-term result of repeated cycling of mirrors between the on and off states. Mirror cycling tests look for hinge fatigue (broken hinges) and failure of the mirrors to release because of increased adhesion (reset failure). To date, in accelerated tests, a lifetime of more than 765 billion cycles has been demonstrated (equivalent lifetime >76,000 hours) for a 10-bit/primary color, three-chip projector configuration).

3.0 DLP SYSTEM DESCRIPTION AND OPERATION

3.1 System design [20, 27, 42].

Figure 13 illustrates a generic three-chip DLP system broken down into its functional components (video front-end, digital processor, digital formatter, and digital display). The generic video front-end accepts a variety of video sources (digital, digital compressed, digital graphics, analog composite, analog s-video, and analog graphics). The video front-end performs the functions of decompression, decoding, and ana-

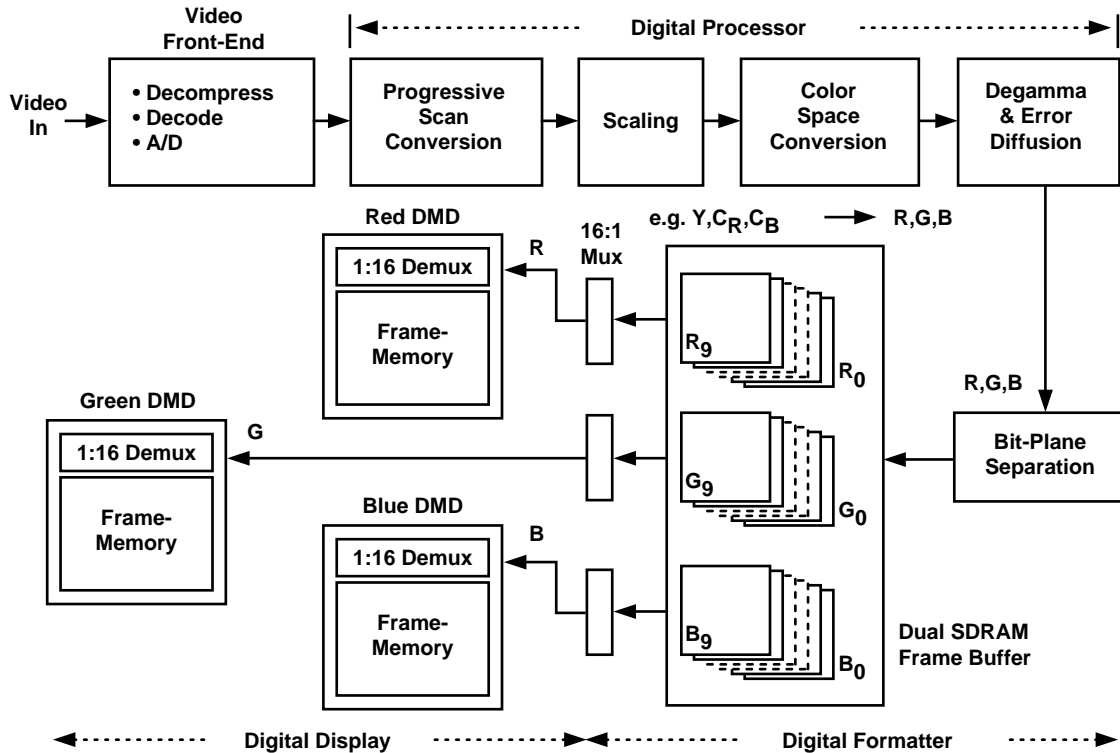


Figure 13. Generic DLP system diagram

log-to-digital conversion, depending on the nature of the video source.

The first operation in the digital processor is progressive-scan conversion. This conversion is required if the original source material is interlaced. An interlaced format provides even lines of video during one video field time and odd lines during the next field time. Progressive-scan conversion is the process of creating (by an interpolation algorithm) new scan lines between the odd or even lines of each video field.

Interlacing has been historically used in CRT-based systems to reduce the video bandwidth requirements without producing objectionable flicker effects created by the temporal decay in phosphor brightness. For progressively scanned CRTs, interlacing is unnecessary because additional bandwidth is allocated so that every line of the CRT is refreshed during each field time. Progressive scanning that incorporates motion-adaptive algorithms helps to reduce interlace scanning artifacts such as interline flicker, raster line visibility, and field flicker. These are particularly noticeable in larger display formats.

The next operation in the digital processor is digital resampling (or scaling). This operation resizes the video data to fit the DMD's pixel array, expands letterbox video sources, and maintains a correct aspect ratio for the square pixel DMD format. After the scaling operation, the video data is input to the color space conversion block. If the video is not already in a red, green, blue (R,G,B) format, it is converted from lu-

minance and color difference encoding (e.g., Y, C_R, C_B) into R,G,B. Next, a degamma (inverse gamma) function is performed because, unlike CRTs, DMDs are linear displays. The degamma operation can produce low-light-level contouring effects, but these are minimized by using an error diffusion technique.

Finally the R,G,B signal is input to the digital formatter. First, the scan-line format data is converted into an R,G,B bit-plane format. The bit planes are stored in a dual-synchronous DRAM (SDRAM) frame buffer for fast access of the bit-plane data. The bit-plane data is then output to the DMDs in a PWM bit-splitting sequence (Section 2.2). As explained in Section 2.4, the DMD chip has multiple data inputs that allow it to match the frequency capability of the on-chip CMOS with the required video data rates. The bit-plane data coming out of the frame buffer is multiplexed 16:1 and fed to the multiple data inputs of each DMD. The bit-plane data is then demultiplexed 1:16 and fed to the frame-memory underlying the DMD pixel array.

3.2 Projection optics [44].

DLP optical systems have been designed in a variety of configurations distinguished by the number of DMD chips (one, two, or three) in the system [44]. The one-chip and two-chip systems rely on a rotating color disk to time-multiplex the colors. The one-chip configuration is used for lower brightness applications and is the most compact. Two-chip systems

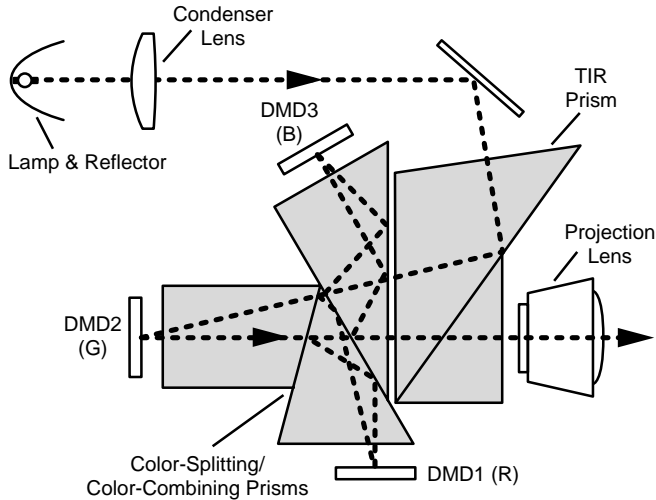


Figure 14. DLP three-chip optical system

yield higher brightness performance but are primarily intended to compensate for the color deficiencies resulting from spectrally imbalanced lamps (e.g., the red deficiency in many metal halide lamps). For the highest brightness applications, three-chip systems are required.

A DLP optical system with three chips is shown in *Figure 14*. Because the DMD is a simple array of reflective light switches, no polarizers are required. Light from a metal halide or xenon lamp is collected by a condenser lens. For proper operation of the DMD light switch, this light must be directed at 20 degrees relative to the normal of the DMD chip (*Figure 6*). To accomplish this in a method that eliminates mechanical interference between the illuminating and projecting optics, a total internal reflection (TIR) prism is interposed between the projection lens and the DMD color-splitting/-combining prisms.

The color-splitting/-combining prisms use dichroic interference filters deposited on their surfaces to split the light by reflection and transmission into red, green, and blue components. The red and blue prisms require an additional reflection from a TIR surface of the prism in order to direct the light at the correct angle to the red and blue DMDs. Light reflected from the on-state mirrors of the three DMDs is directed back through the prisms and the color components are recombined. The combined light then passes through the TIR prism and into the projection lens because its angle has been reduced below the critical angle for total internal reflection in the prism air gap.

A DLP three-chip prototype projection engine is shown in *Figure 15*. It projects 1100 lumens with a 500-watt xenon lamp. The size of the engine is 19.5 × 12.8 × 10 in. and it weighs 38 pounds. One of the DMD package assemblies with thermoelectric cooler and fan is visible.

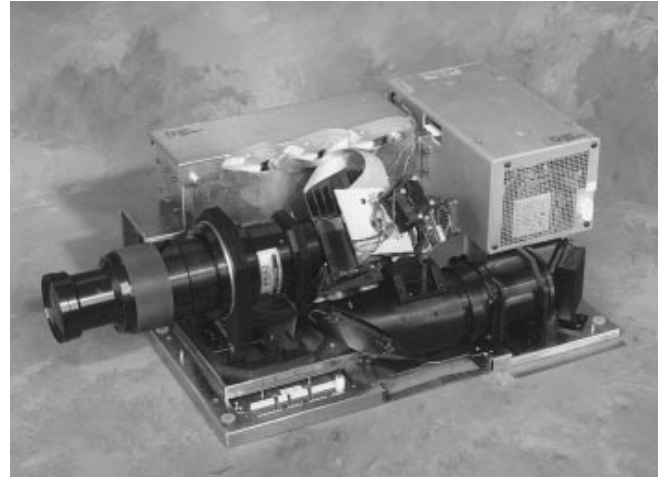


Figure 15. DLP three-chip prototype projection engine

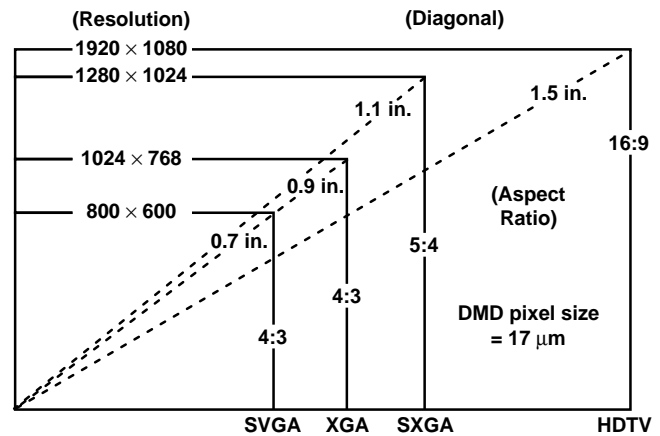


Figure 16. DMD resolution versus chip diagonal

4.0 DISPLAY PERFORMANCE

4.1 Resolution

DLP projection systems have been demonstrated at a variety of resolutions (and aspect ratios), VGA (640 × 480), SVGA (800 × 600) and SXGA (1280 × 1024). A 16:9 aspect ratio high-definition (1920 × 1080) DLP projection system has also been demonstrated [20, 27, 35]. Currently there are DLP-based products on the market for business applications at SVGA resolution. Both professional (high-brightness) and business products will be available at XGA resolution by the end of 1997. SXGA products will follow in 1998.

The DMD family of chips uses a common pixel design having a 16 μm mirror arrayed with a 17 μm pixel pitch. As the DMD resolution is increased, the pixel pitch is held constant and the chip diagonal is allowed to increase (*Figure 16*). This approach to the chip design has several advantages: (1) the high optical efficiency and contrast ratio of the pixel is maintained at all resolutions, (2) pixel timing is common to all

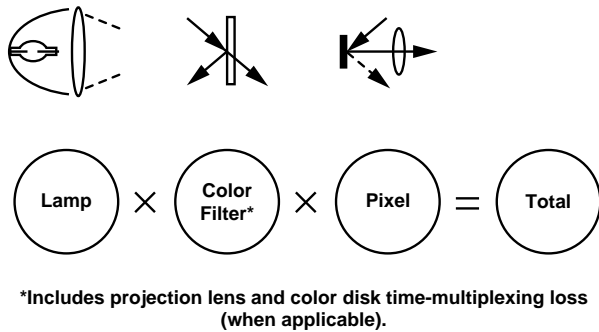


Figure 17. Optical efficiency of DLP projection system

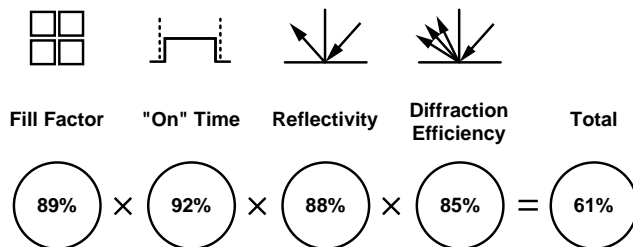


Figure 18. Optical efficiency of DMD pixel

designs and high address margins are maintained, and (3) the chip diagonal increases with resolution, which improves the DMD system optical efficiency (see Section 4.2).

4.2 Optical efficiency and brightness

The optical efficiency of the DLP projection system is the product of the efficiencies shown in *Figure 17*, namely the lamp/reflector, color filter/projection lens, and pixel efficiencies.

The pixel efficiency is composed of the product of the efficiencies shown in *Figure 18*, namely the fill factor, mirror “on” time, reflectivity, and diffraction efficiency. For the DMD pixel design used today, the pixel efficiency is 61% [44].

The color filter/projection lens efficiency depends on the dichroic filter reflection and absorption losses and reflection losses in the projection lens elements. For one-chip or two-chip DMD systems that use a rotating color disk, there is an additional loss associated with the time-multiplexing of the colors.

The lamp/reflector efficiency depends on the amount of collected light that can be used by the DMD: This is a function of the arc length of the lamp, the reflector geometry, the area of the mirror array, and the cone angle ($f/\#$) of the illumination and projection lens.

To understand the relationship of these parameters and their influence on the lamp/reflector efficiency, it is useful to use the concept of *etendue*, which is also known as “optical extent” or the “optical invariant.” *Etendue* is a measure of the

area of the light distribution, convolved with the solid angle of the light [60].

When a beam is modified by a well-corrected optical element, *etendue* is preserved. For example, when a well-corrected lens focuses a collimated beam to a spot, the area of the beam is reduced, but the divergence angle of the beam increases and *etendue* is preserved. The lamp/reflector combination has an *etendue*. The DMD/projection lens combination also has an *etendue*. If the *etendue* of the DMD/projection lens is smaller than that of the lamp/reflector, then the system is said to be *etendue*-limited. In this case, not all of the collected light from the lamp/reflector can be used by the DMD/projection lens. This is the case for all lamps but those with the shortest arc lengths.

To maximize the lamp reflector efficiency, it is necessary to minimize the *etendue* of the lamp in relation to that of the DMD/projection lens. The *etendue* of the DMD/projection lens is given by $E = \pi A/4f^2$, where A is the area of the DMD and f is the $f/\#$ of the projection lens. The $f/\#$ of the projection lens for the DMD is determined by the mirror rotation angle of ± 10 degrees. To adequately separate the on-state light from the diffracted light produced by the mirror edges and substrate and to maximize contrast ratio, an $f/\#$ no smaller than $f/2.8$ is required. To preserve adequate contrast ratio in the resulting projected image, the DMD projection lens is typically fixed at $f/3.0$. Thus the DMD/projection lens *etendue* is determined solely by the area (resolution) of the DMD and increases with resolution.

For a given resolution DMD, the lamp/reflector efficiency *increases* as the lamp arc length (and *etendue*) *decreases*. For this reason, short arc length lamps (<2 mm) are chosen for DLP applications. For a given lamp *etendue*, the lamp/reflector efficiency *increases* as the resolution (and *etendue*) of the DMD *increases*. This latter relationship is shown graphically in *Figure 19*, where the modeled optical efficiency (lumens/watt) of DLP three-chip projectors is shown plotted versus DMD resolution for lamps of various powers. The SVGA resolution optical efficiencies (for the 500- and 900-watt lamps) are actual measurements from prototype projectors. Also shown is the total luminous flux in lumens that can be delivered at SVGA resolution.

For lower lamp power (lower brightness applications), the highest optical efficiencies are achieved with metal halide (MH) lamps because of their high luminous efficacy. However, as the lamp power is increased, the arc length of metal halide lamps must grow more rapidly than that of xenon (Xe) lamps to preserve lamp lifetime (typically determined by the time for the brightness to diminish to 50% of the stabilized brightness of a new lamp). Therefore, in DLP applications (for power levels above ~300 watts), xenon lamps, because of their shorter arc, provide better lamp/reflector collection efficiencies and higher overall system performance.

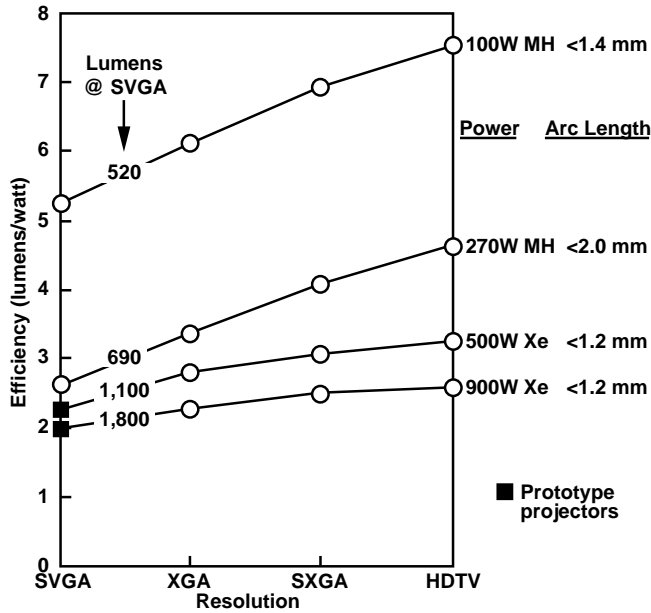


Figure 19. Modeled optical efficiency (lumens/watt) versus resolution for DLP three-chip projectors

It should be noted that a large color gamut and good color balance (particularly for flesh tones) are important in high-brightness applications such as digital cinema. Although metal halide lamps have a higher efficacy (lumens/watt) compared to xenon, not all of the luminous output can be used if color balance is to be preserved. Most metal halide lamps are typically characterized by having strong green (mercury) and greenish yellow (sodium) emission lines. These lines carry a significant portion of the lamp's luminous output. However, for proper color balance, these lines must be attenuated, with a resulting drop in the effective efficacy of the lamp.

Often it is difficult to compare projection system performance (in terms of optical efficiency) of systems using xenon lamps versus those that use metal halide lamps. Unless the color balance for these systems is adjusted to the same specification (e.g., SMPTE-C RGB points and a D65 luminant color balance), the luminous output of metal halide systems will naturally be overstated. Therefore, the lamps of *Figures 19* and *20* have been color-balanced to achieve a valid comparison of their performance.

In *Figure 20*, the modeled brightness (lumens) of DLP three-chip projectors is plotted versus DMD resolution for lamps of various powers. For the 500-, 900-, and 1,500-watt lamps, the SVGA resolution brightness levels are actual measurements from prototype projectors. Brightness levels up to 3000 lumens at SVGA resolution have been demonstrated with short arc xenon lamps. The modeled performance at HDTV resolutions with current lamps is projected to be 3600 lumens. With further improvements in short-arc xenon lamp technol-

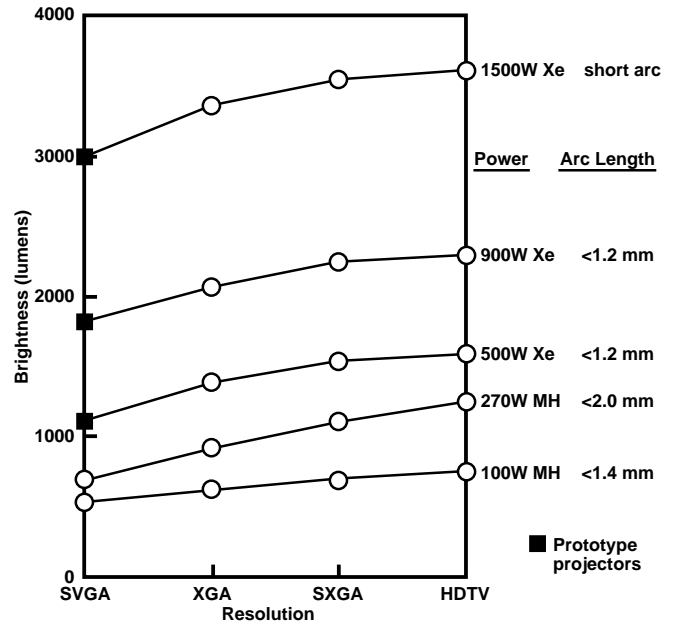


Figure 20. Modeled brightness versus resolution for DLP three-chip projectors

ogy, Digital Projection Ltd. (formerly Rank-Brimar) anticipates that brightness levels in excess of 10,000 lumens will be achieved in DLP brand products as resolution and format approach HDTV standards.

4.3 Maximum brightness

At high luminous flux densities (lumens/cm²), optical absorption creates heating effects. Excessive temperature can cause degradation of performance for both LCDs and DMDs. In the case of LCDs, excessive heating causes degradation of the polarizers. Furthermore, without adequate cooling of the LCD panel, the temperature of the LCD material can rise above its clearing temperature T_c . This renders the LCD material useless for polarization rotation and the display fails. For transmissive AM-LCD panels, a heatsink cannot be attached to the substrate, so forced air cooling must be relied upon. Larger transmissive panels mitigate this problem. Currently, AM-LCD projectors having 3000-lumen outputs use 5.8 × 5.8 in. panels.

Excessive temperatures can also affect the long-term reliability of the DMD by accelerating hinge deformation (metal creep) that can occur under high-duty-factor operation of the mirror. Special hinge alloys have been developed to minimize this deformation and guarantee reliable operation [52]. High duty factors occur when the mirror is operated in one direction for a much greater part of the time, on average, than in the other direction. For example, 95/5 duty factor operation means that a mirror is 95% of the time at one rotation angle (e.g., -10 degrees) and 5% of the time at the other rota-

tion angle (e.g., +10 degrees). This situation would correspond to DMD operation with a video source having a temporal average brightness of 5% (or 95%) of the peak brightness. Although these extreme temporal averages are unlikely to occur for extended periods of time, 95/5 duty factor is chosen as a worst case reliability test condition for hinge deformation. With current hinge metal alloys, long-term, reliable DMD operation at the 95/5 duty factor is assured, provided the operating temperature of the hinge is limited to <65°C.

For high-brightness applications, the mirrors can absorb enough energy to raise the hinge temperature above 65°C unless active cooling is applied to the package. Because the DMD is reflective and built on a single-crystal silicon (X-silicon) backplane, the absorbed heat can be efficiently extracted by connecting a thermoelectric cooler (TEC) to the backside of the DMD package. In *Figure 15*, one of the DMD package assemblies with the thermoelectric cooler is visible. The DMD package contains a “thermal via” to provide a low-thermal-impedance path between the DMD chip and the TEC. A thermal model predicts that for a three-chip SXGA projector producing 10,000 screen lumens, the hinge temperature can be held to <65°C (with TEC cooling and an internal ambient air temperature of 55°C).

4.4 Contrast ratio

The inherent contrast ratio of the DMD is determined by measuring the ratio of the light flux with all pixels turned on versus the flux with all pixels turned off. The system contrast ratio is determined by measuring the light flux ratio between bright and dark portions of a 4 × 4 checkerboard image according to ANSI specifications. The checkerboard measurement takes into account light scatter and reflections in the lens, which can degrade the inherent contrast ratio of the DMD.

The full on/off contrast ratio determines the dark level for scenes having a low average luminance level (e.g., outdoor night scenes) as well as the video black level. The checkerboard contrast ratio is a measure of the contrast for objects in scenes containing a full range of luminance levels.

The inherent contrast ratio of the DMD is limited by light diffraction from the mirror edges, from the underlying substrate, and from the mirror via (the metallized hole in the middle of the mirror that acts as the mirror support post, as shown in *Figure 4*). Recent architectural improvements to the DMD pixels have led to improved contrast ratios (*Table 2*) [61]. Further improvements are expected.

4.5 Accuracy and stability

Current high-brightness projection displays for use in the audio/visual rental and staging business and for private and corporate use have a number of limitations. These include warmup or stabilization time; setup time for convergence,

Table 2. Contrast ratio for standard and improved pixel architecture in a prototype system

	Original Design	New Design
Full on/full off	255:1	370:1
Checkerboard (4 × 4)	142:1	177:1
Note: All data for f/3.0 projection lens.		

color balance, and gamma; and, finally, the stability of the image quality once the system is operating. Maintaining stability over a wide range of environmental conditions encountered in outdoor applications is particularly difficult. For video wall applications or other applications requiring multiple side-by-side projectors, the setup time to make all of the displays look identical is often unacceptable. Even when great care has been taken in this procedure, lack of stability makes periodic adjustments necessary.

DLP-based projection systems offer the potential of short setup time and stable, adjustment-free images. Initial stabilization time is minimal. Convergence is fixed by internal alignment of the three DMDs and is stable with time and independent of throw distance. Color balance, uniformity, and gamma are digitally controlled by pulsewidth modulation and are not affected by temperature. Brightness rolloff is stable (fixed by a light integrator) and can be made small to accommodate video wall applications.

5.0 DLP BRAND PRODUCTS

Texas Instruments is teamed with numerous projection display manufacturers spanning the business (conference room), consumer (home theater), and professional (high-brightness) markets [62]. DLP brand products and prototypes serving all three market segments have been demonstrated at numerous trade shows including Cedia, Comdex, CES, Infocomm, EID, IFA, JES, Photokina, Photonics West, SID, and Satis. Shipments of the first DLP brand business projectors began in March 1996. Soon the first consumer and professional products will be available on the market.

Currently, Digital Projection Ltd., Electrohome, and Sony are developing high-brightness DLP brand products with SVGA resolution and brightness levels ranging from 1100 lumens to 3000 lumens. Announcements of the first DLP brand professional products is expected in the first quarter of 1997.

6.0 SUMMARY

DLP brand projection displays are well-suited to high-brightness and high-resolution applications. The digital light switch is reflective and has a high fill factor that results in high optical efficiency at the pixel level and low pixelation effects in the projected image. The DMD family of chips uses a common pixel design and a monolithic CMOS-like process. These

factors, taken together, mean that scaling to higher resolutions is straightforward, without loss of pixel optical efficiency. At higher resolutions, the DLP brand projector becomes even more efficient in its use of light because of higher lamp-coupling efficiency. Because the DMD is a reflective technology, the DMD chip can be effectively cooled through the chip substrate, thus facilitating the use of high-power projection lamps without thermal degradation of the DMD. DLP brand systems are all-digital (digital video in, digital light out) that give accurate, stable reproduction of the original source material.

DLP brand projectors for the business (conference room) application are currently on the market. Soon, the first consumer (home theater) products will be available. DLP brand projection system prototypes for professional (high-brightness) applications have been demonstrated at up to 3000-lumen brightness for SVGA resolution. Soon, high-brightness SVGA products will be on the market, followed by XGA and SXGA products. With anticipated improvements in short-arc xenon lamp technology, it is expected that brightness levels in excess of 10,000 lumens should be achievable in DLP brand products of the future, as resolution and format approach HDTV standards.

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